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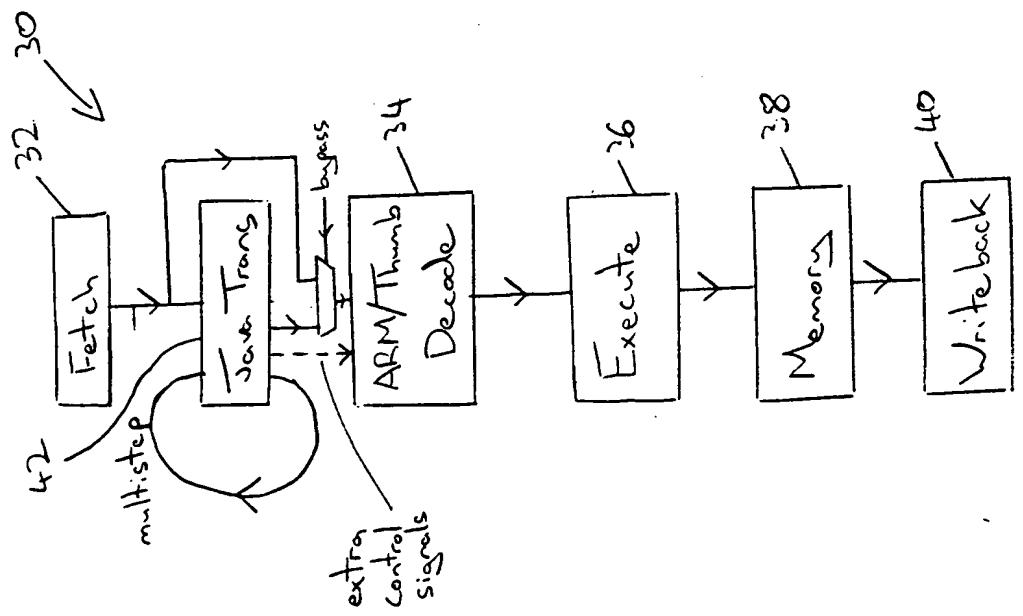


Fig. 1

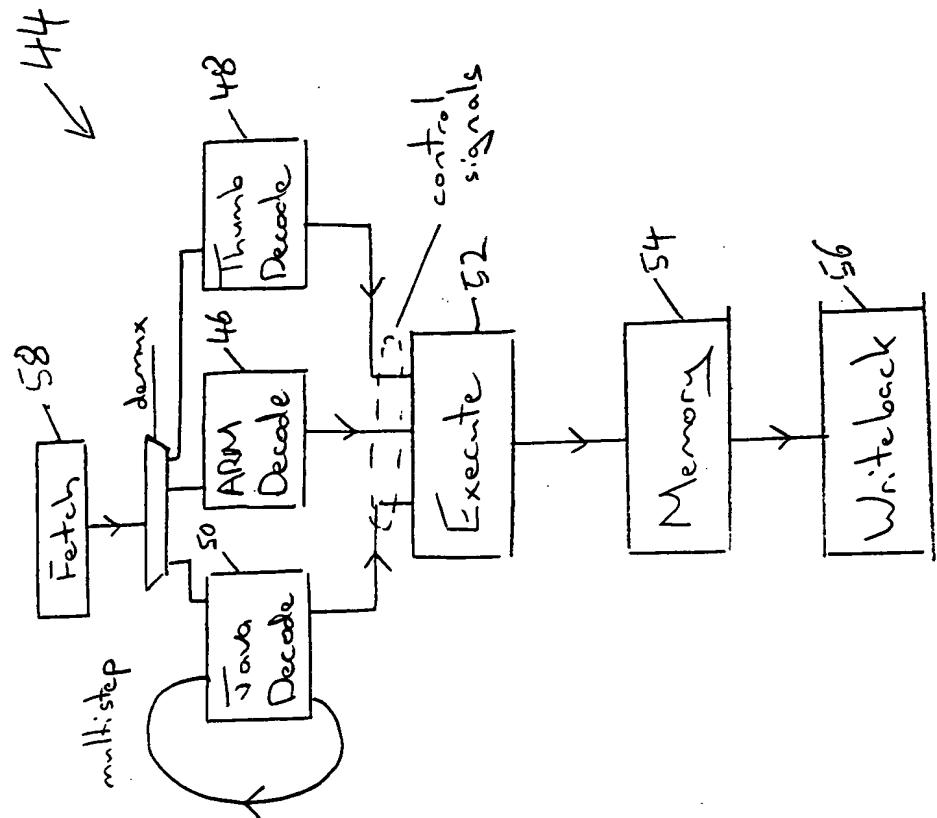


Fig. 2

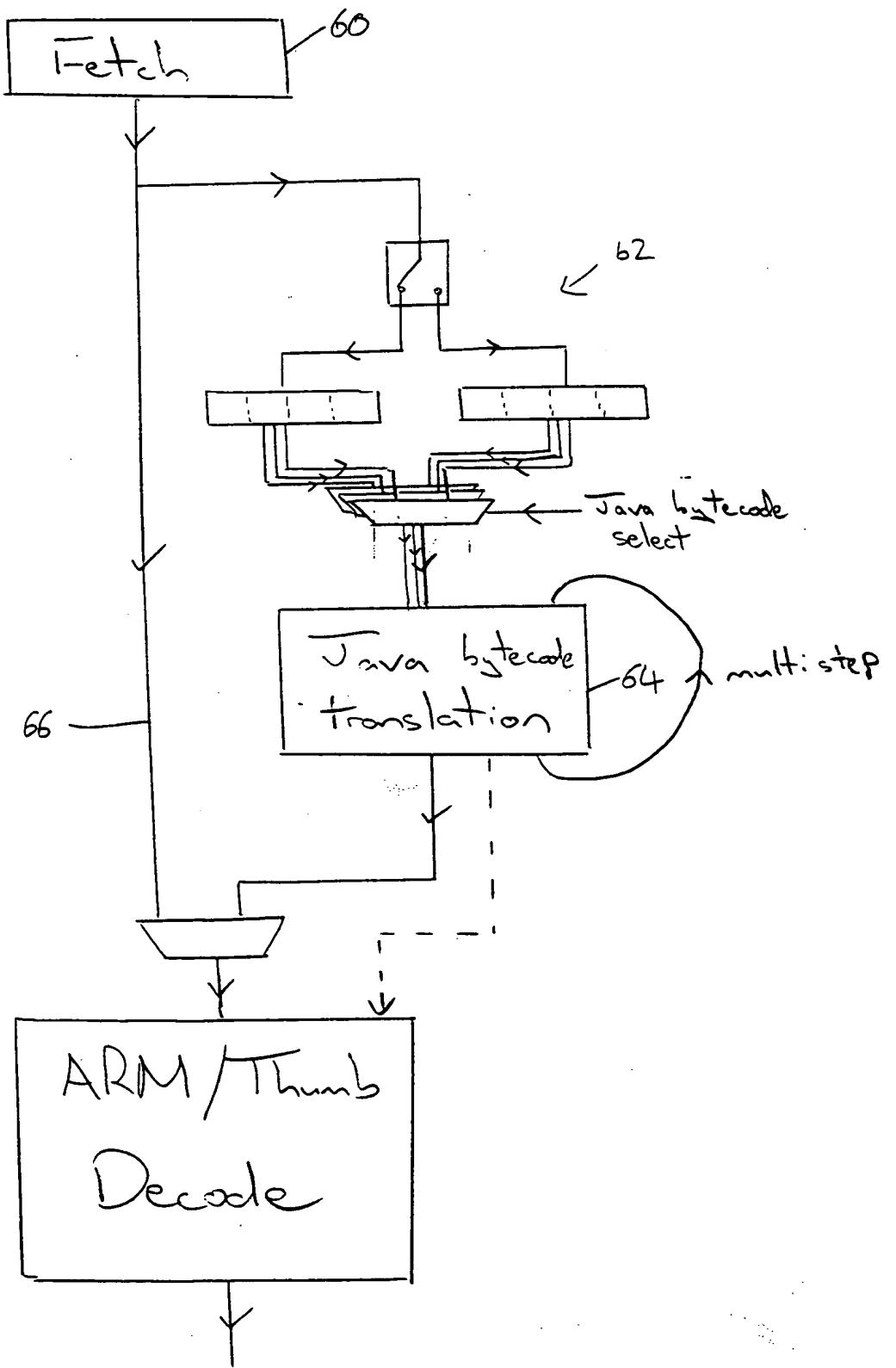


Fig. 3

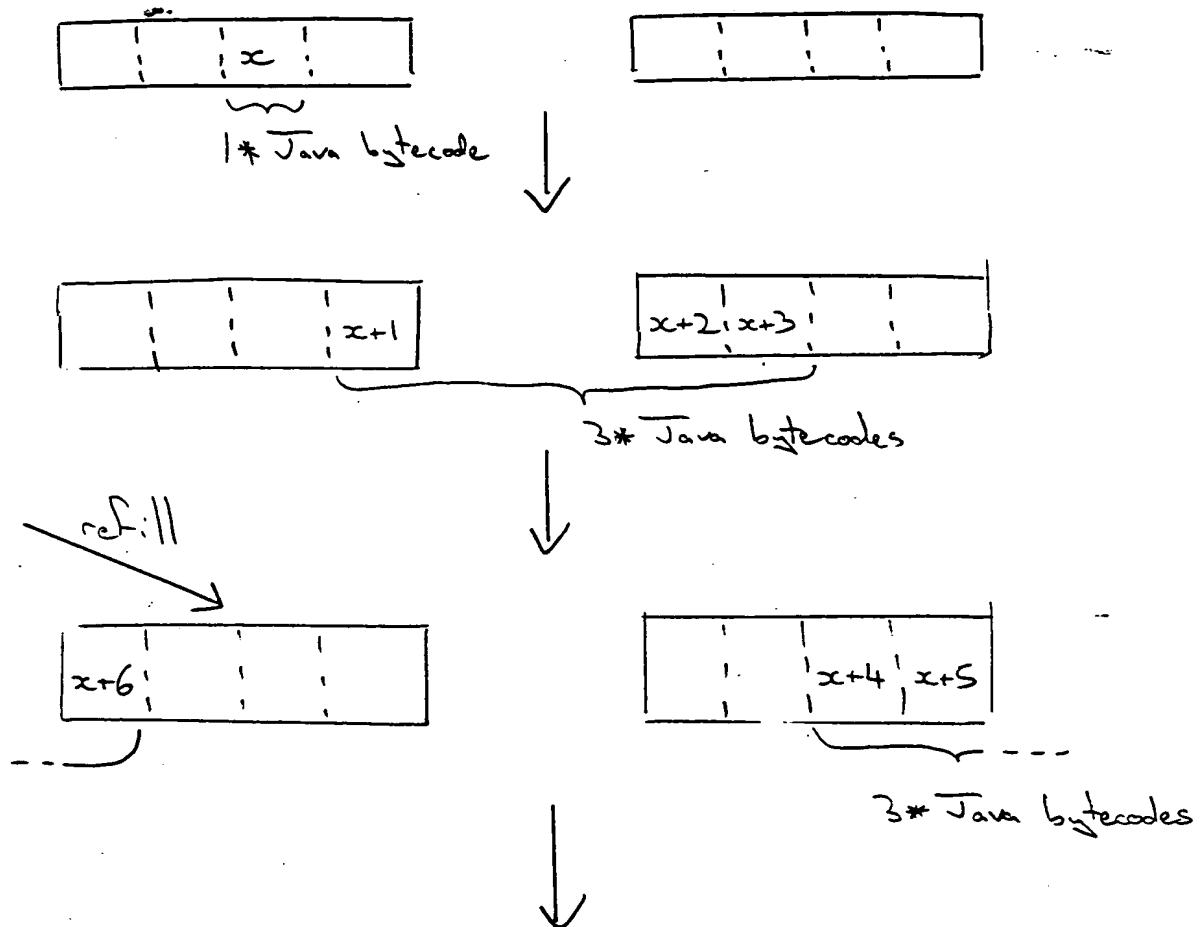


Fig. 4

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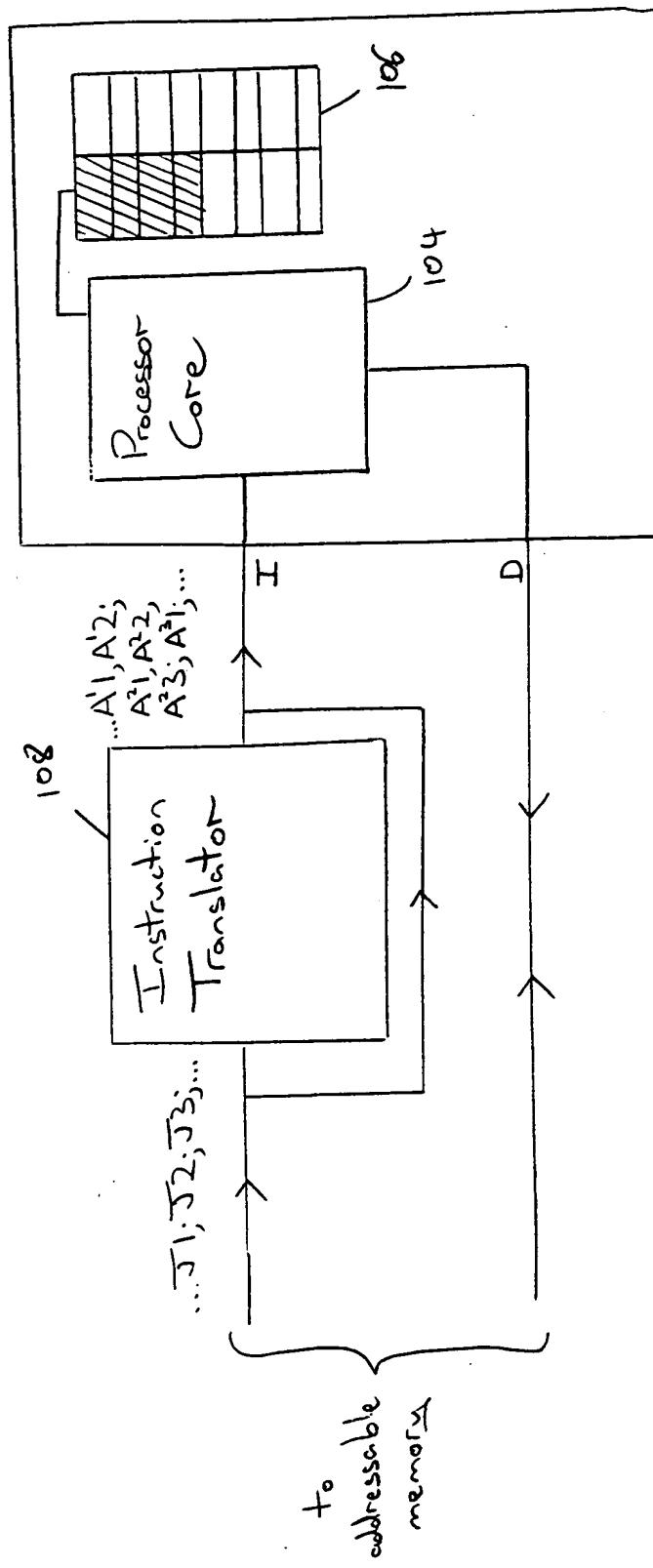


Fig. 5

Fig. 6

Load

RF = 2	SA = 0
RE = 2	(swap)

01001	TOS-1	Index	Array Ref

LDR R12,[R0,#0]
 LDR R2,[R2,R1],LSL#3]

E E

01001	TOS-1	Index	Array Ref

E E

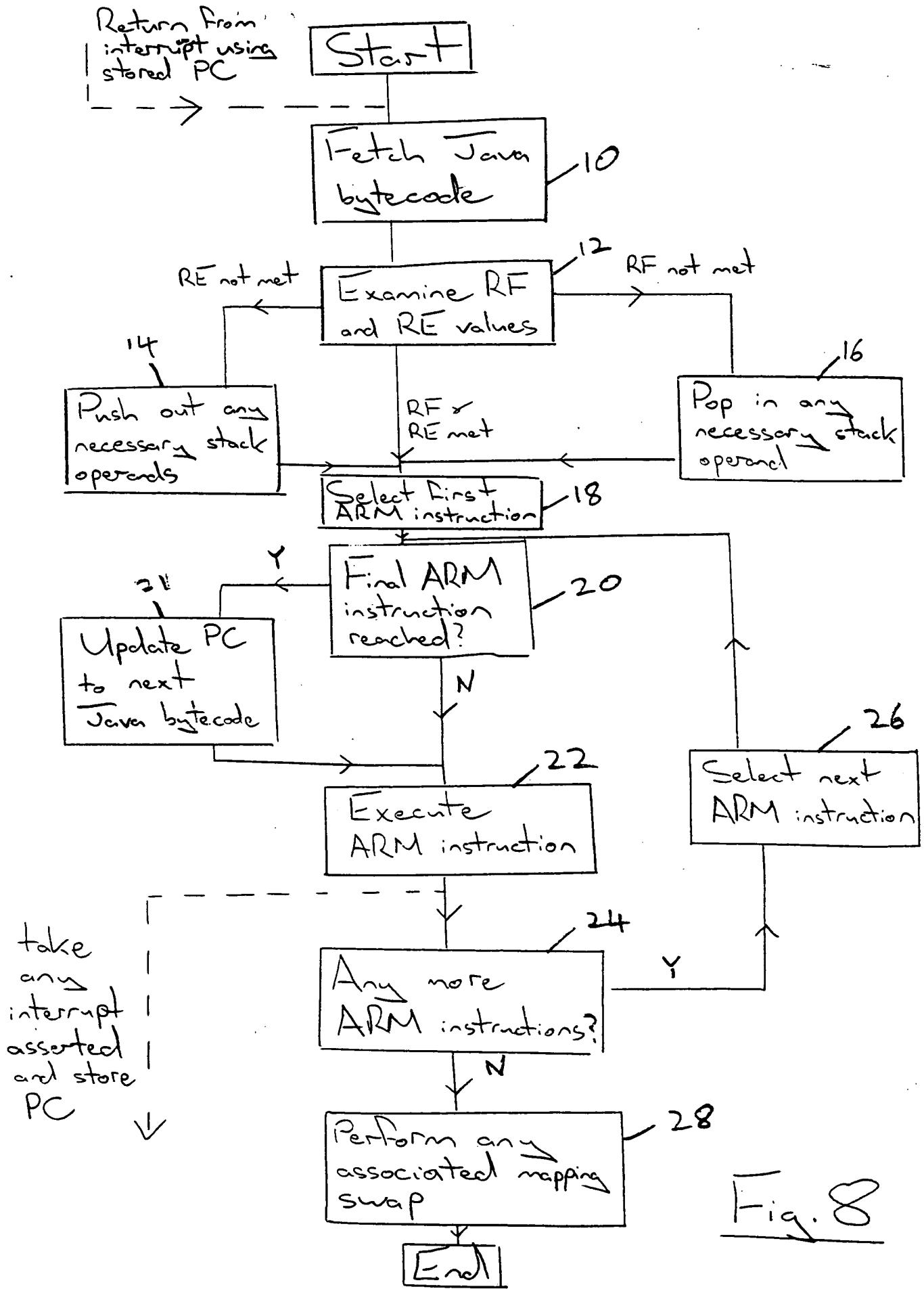
01011	E	E	Array Ref

LDR R3,[R12,#4]
 (state swap)

E E

TOS-1 TOS
 1st Array Word 2nd Array Word

Fig. 7



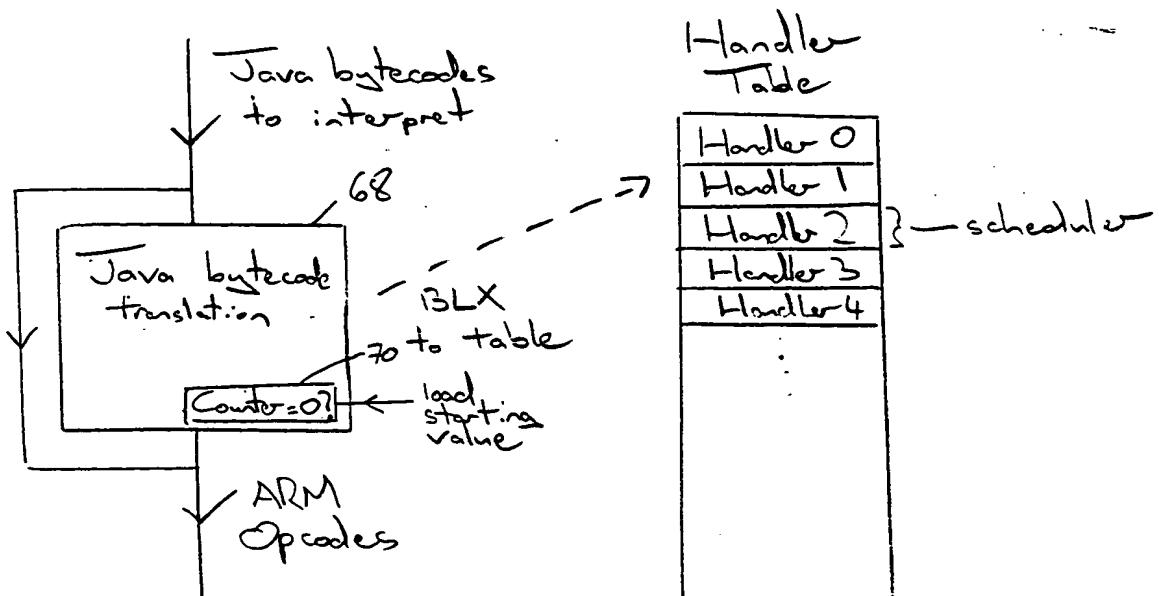


Fig. 9

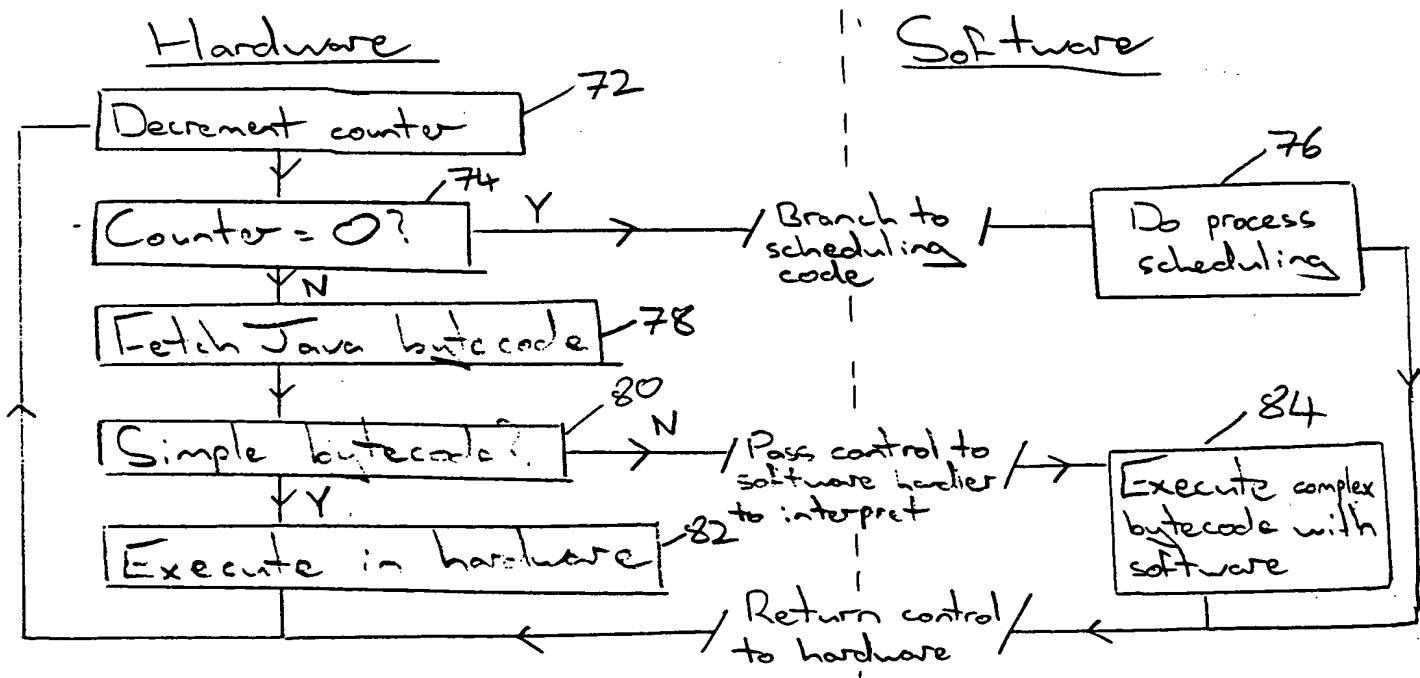
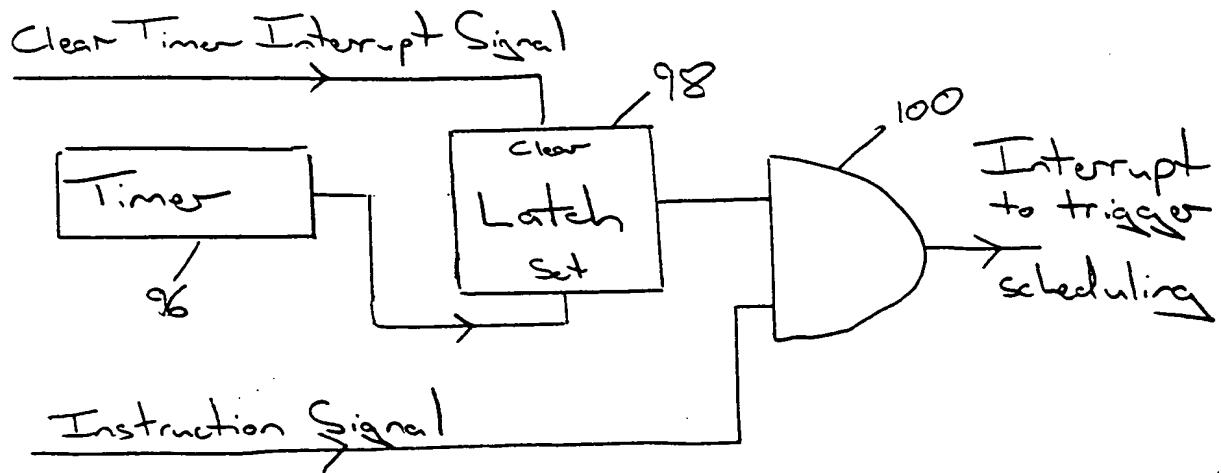
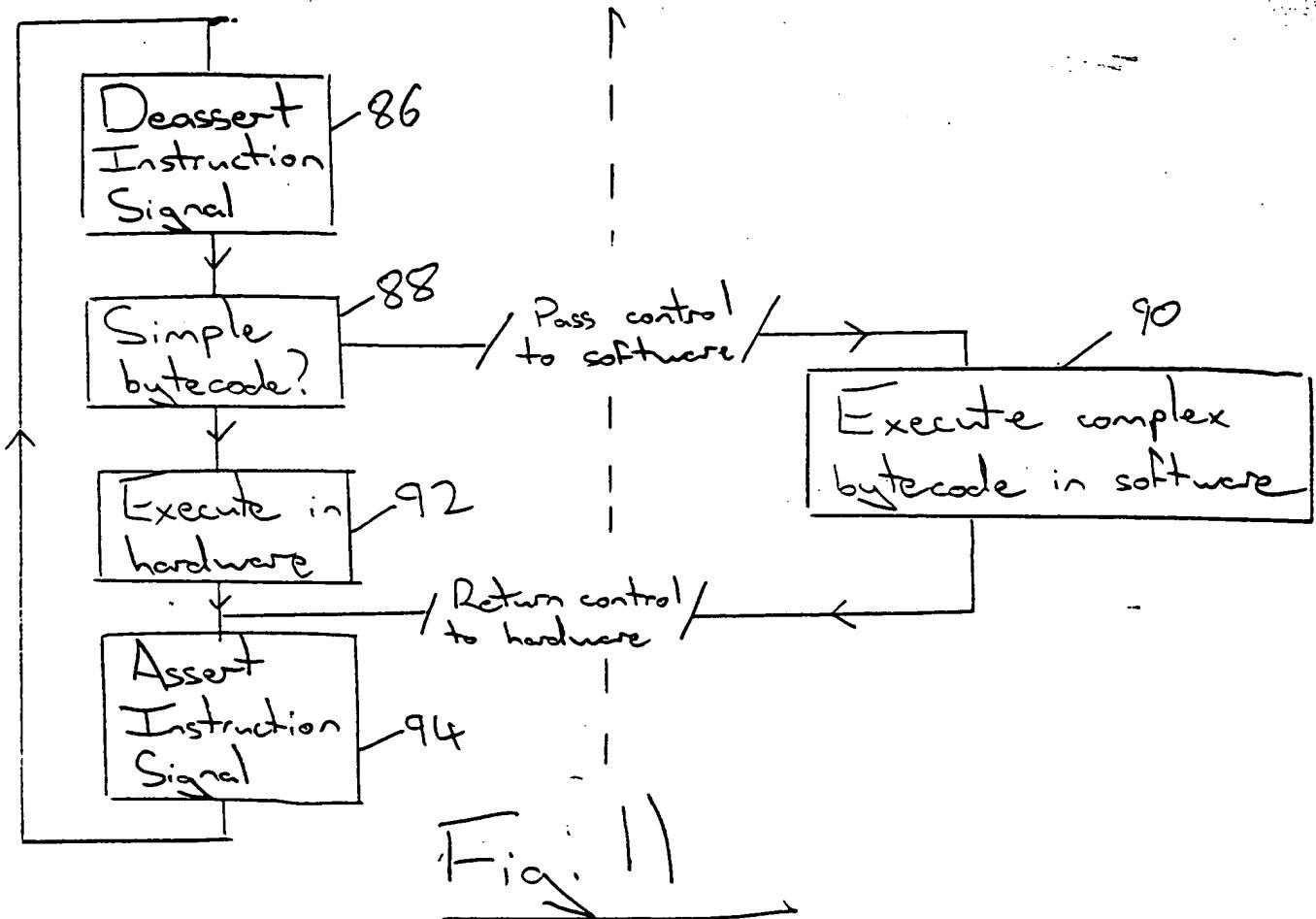


Fig. 10

Hardware

Software





Core
Clock



Timer



Latched
Timer



Instruction



Interrupt



Clear
Interrupt

Fig. 13